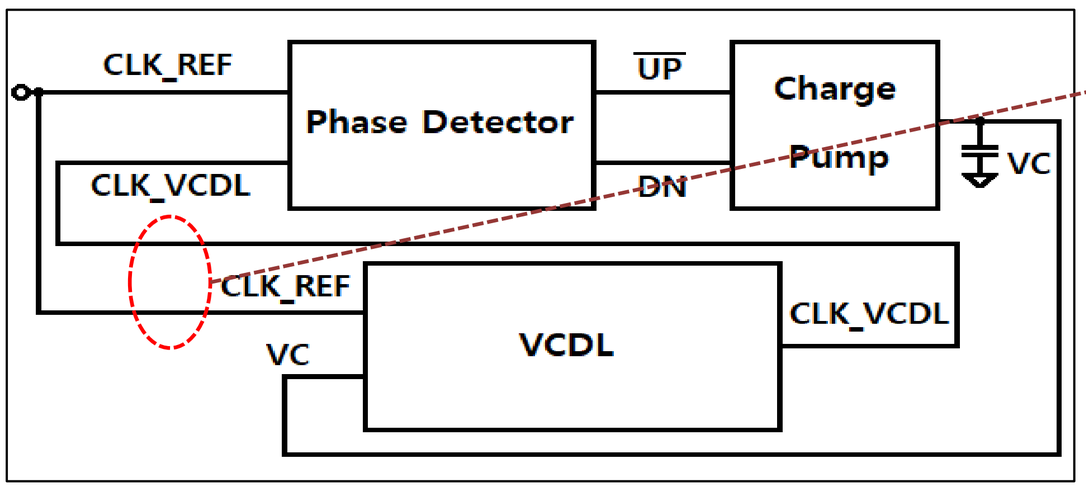
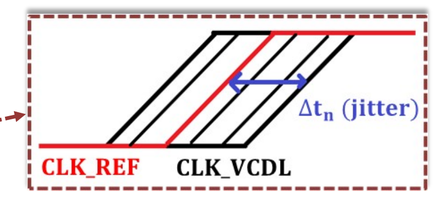
Study on Jitter Analysis and Reduction Methods in DLL

Jin-Won Hyun, Jae-Yoon Kim, Seung-Jae Kim and Jae-Won Nam

Introduction



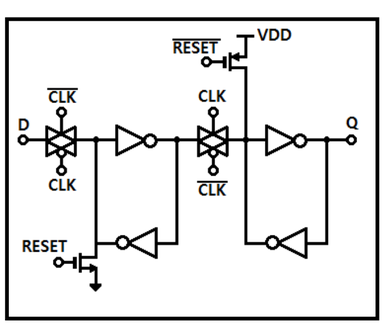


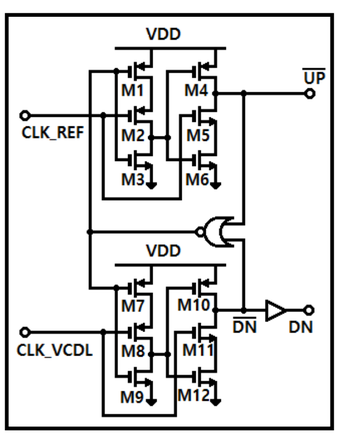
$$\Delta t_{n,rms} = \sqrt{\sum \frac{(\Delta t_n)^2}{n}}$$

- DLL & PLL are one of the most essential block for clock synchronization or generation. Due to reduced supply voltage, low output jitter is highly required.
- In this work, we designed DLL circuit due to relatively ease than PLL circuit. we applied several methods to reduce jitter under 65nm tech, 1.2V supply voltage.

Method (1)

- **Phase detector**
  - Change Phase detector (MS-DFF PD → TSPC PD)





	MS-DFF	TSPC
RJ [ps]	0.71	0.87
DJ [ps]	15.89	1.79
FoMJ* [dB]	-208.34	-229.95

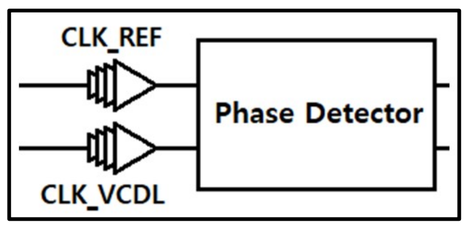
Jitter Reduction Methods

Analysis of jitter contribution → Change phase detector structure → Compensate switching signal's transition time → Optimized W/L

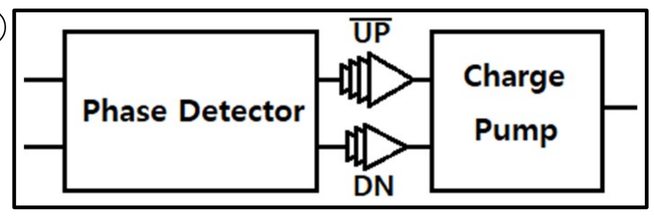
Method (2)

- **Accelerate transition time**
  - -> Added Fan-out-4 buffer

①



②

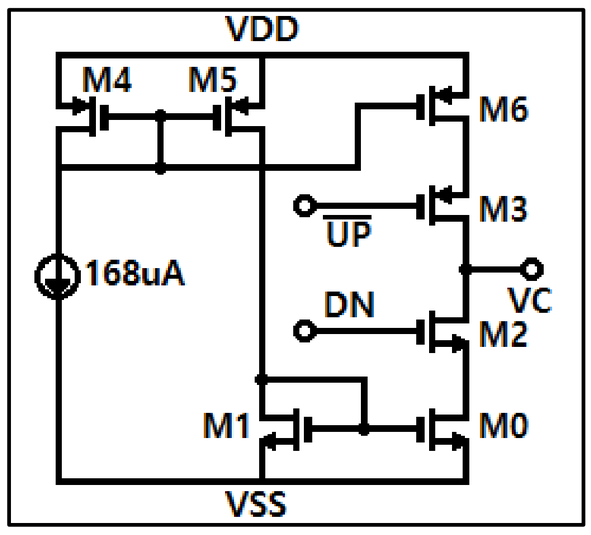


	TSPC	①	②
RJ [ps]	0.87	0.95	0.79
DJ [ps]	1.79	1.02	0.87
FoMJ* [dB]	-229.95	-234.68	236.22

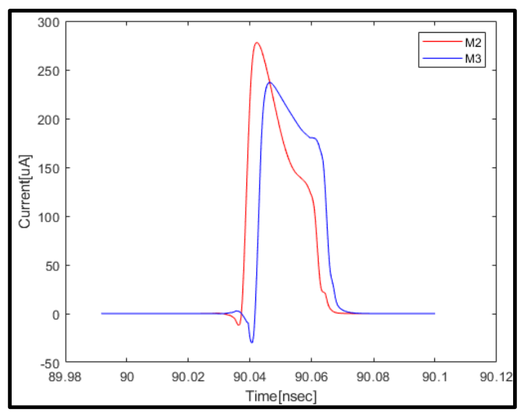
Method (3)

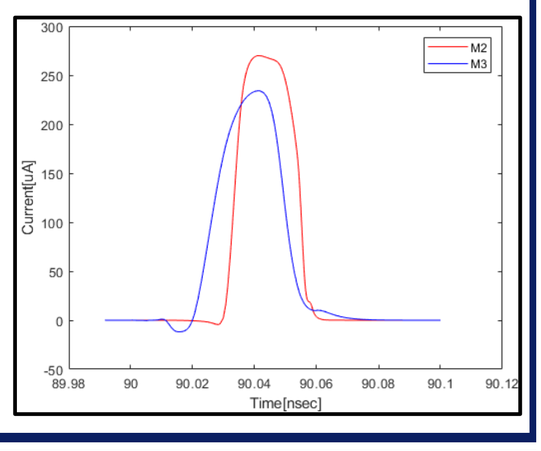
- **Optimized W/L on charge pump**
  - enhancement on charge/discharge current transition time

③



	TSPC	③
RJ [ps]	0.87	0.91
DJ [ps]	1.79	1.22
FoMJ* [dB]	-229.95	-233.16





Overall Simulation Results

	MS-DFF	TSPC	①	②	③	①+②+③+TSPC
RJ [ps]	0.71	0.87	0.95	0.79	0.91	0.648
DJ [ps]	15.89	1.79	1.02	0.87	1.22	0.65
Duty-Cycle [%]	50.4	49.82	49.99	49.75	49.75	49.92
Power [mW]	5.792	3.156	3.275	3.158	3.245	3.274
FoMJ* [dB]	-208.34	-229.95	-234.68	236.22	-233.16	-238.59

$$* \mathbf{FoM_J} = 10 \log\left[\left(\frac{\sigma_t}{1s}\right)^2 \cdot \left(\frac{P_{DC}}{1mW}\right)\right]$$

Future Work

- By comparing various structures of Component Blocks, we can choose optimal blocks for low jitter.
- By adding several Compensation Circuits such as voltage regulator, BGR, we will make output signal robust under PVT variations.

Acknowledgement: This research was financially supported by Seoul National University of Science and Technology, and the MSIT(Ministry of Science and ICT), Korea, under the ITRC(Information Technology Research Center) support program (IITP-2022-RS-2022-00156295) supervised by the IITP. The EDA tool was supported by the IC design education center (IDEC), Korea.