Analysis on Efficiency of DC-DC Converter through Power-Loss Modeling

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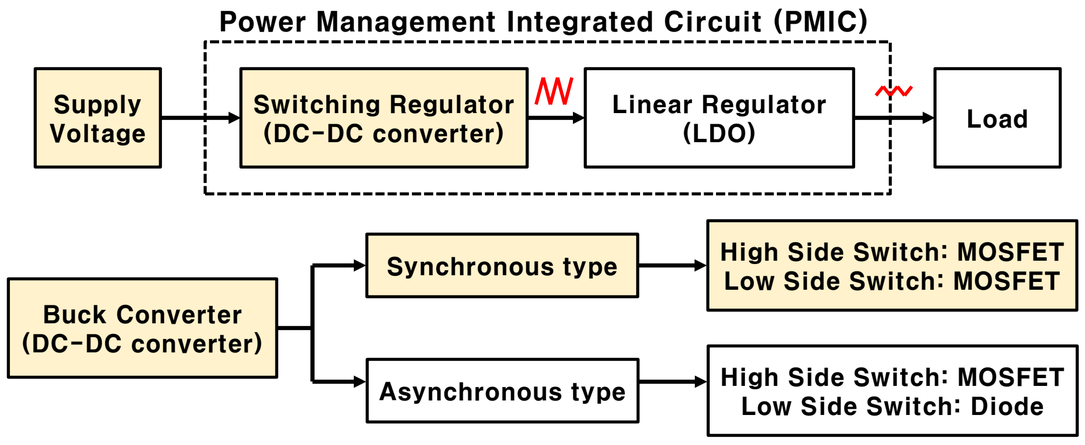
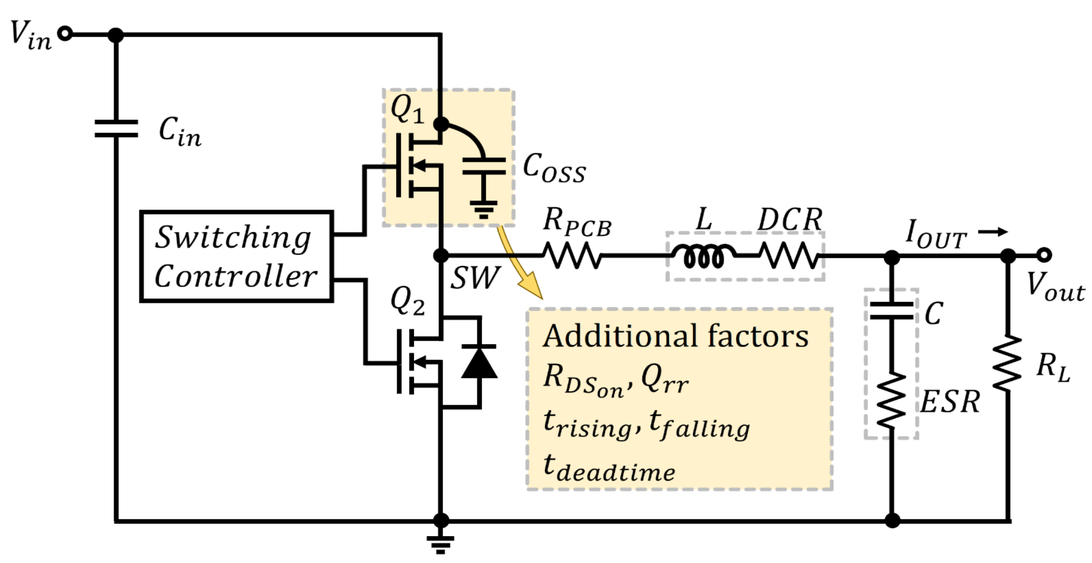
● Introduction & Objectives



◆ Technical Issues

- **Power efficiency** of the buck converter is affected by the power MOSFET, the output stage, the controller, the feedback loop, and the PCB layout, etc.
- Since the performance of the output stage greatly affects the overall performance of the converter, it is important to **optimize** the inductance and capacitance.

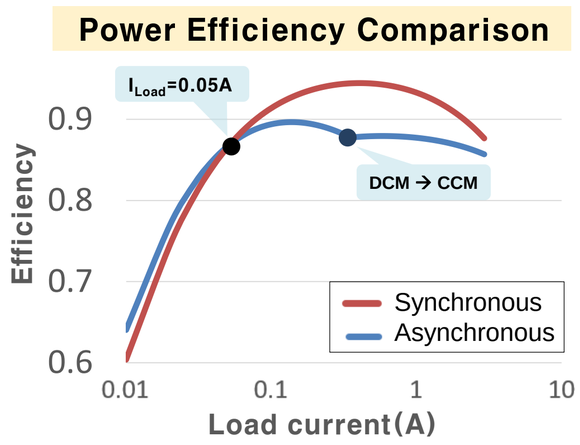
● Concept of Modeling

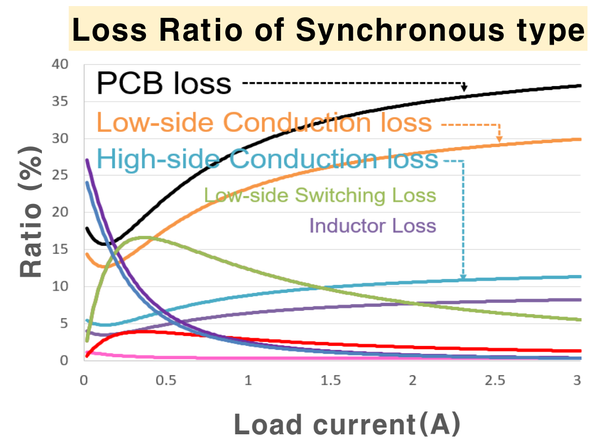


(1) Build a high-level behavior model on MATLAB
(2) Loss Analysis can be done with parameters

● Analysis on Power Efficiency

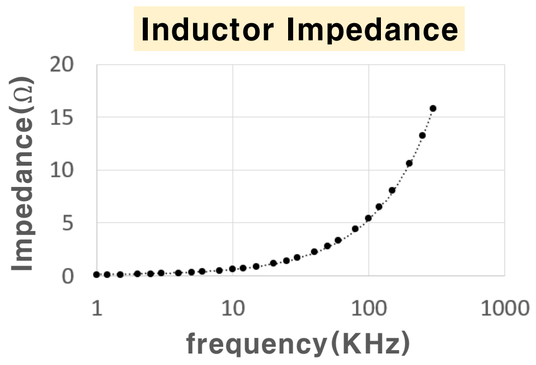
(1) Loss analysis of Synchronous & Asynchronous

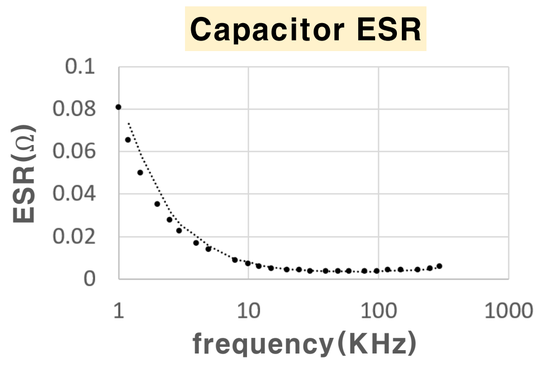




- Synchronous is more efficient @ Heavy load
- Dominant loss is PCB loss(37% @I_{LOAD}=3A)

(2) LCR meter measurement results



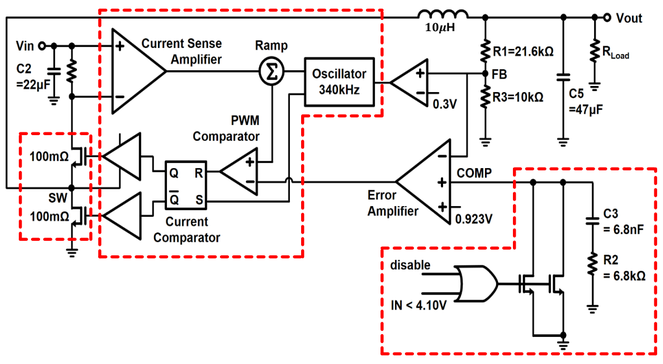


- Extrapolated L, C values at Q-point
  → L=8.34μH, ESR=6mΩ @340kHz
  (∵ Due to a wrack of LCR meter's BW)

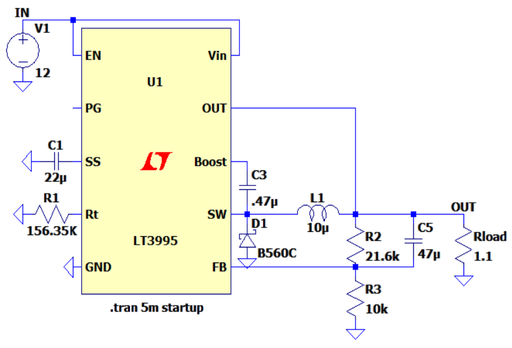
● Simulation & Measurement

(1) SPICE Simulation of Buck Converter

Block Diagram



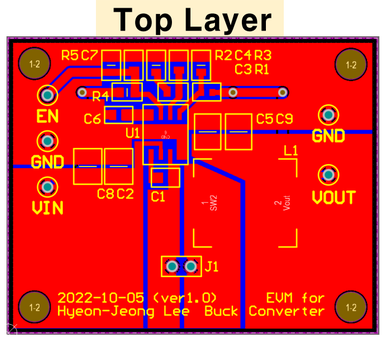
Schematic



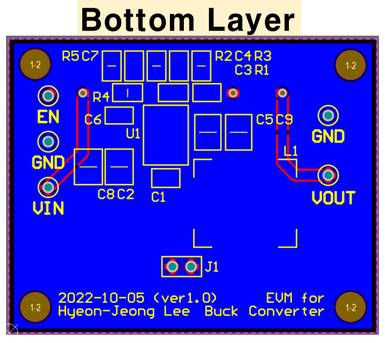
- Synchronous-type Buck Converter
- Current-mode feedback system
- Phase margin = 87.9° @ I_{load}=3A

(2) Measurement based on PCB board

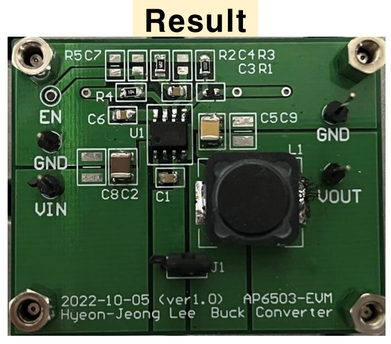
Top Layer



Bottom Layer



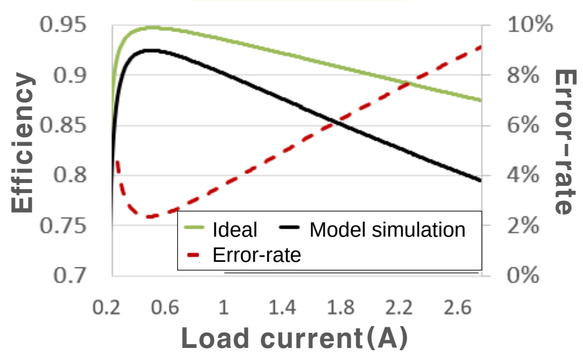
Result



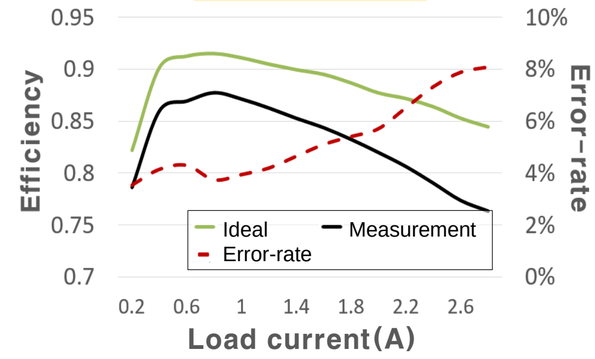
- PCB layout lowering parasitic components
- Probe was grounded with GND wire wrapped

(3) Comparison of modeling and measurement

Modeling



Measurement



● Future work

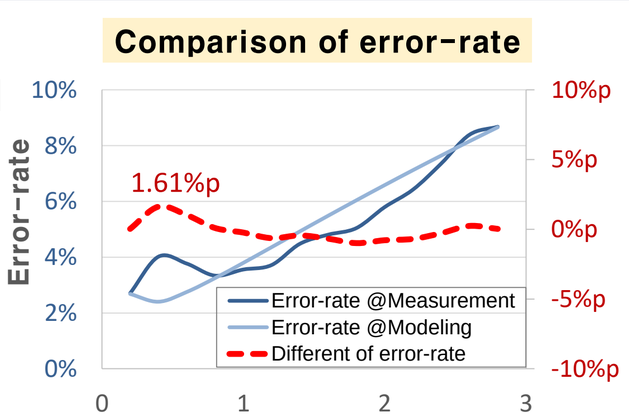
(1) Ripple reduction algorithm based on the model

● Conclusion

✓ Reliability is achieved by comparing loss model with actual measurement

✓ Max error = 1.61%p

Comparison of error-rate



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