ICEIC 2023

Analysis of ROM-based DDFS Architecture Employing Quarter Method

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Introduction

❖ **DDFS**

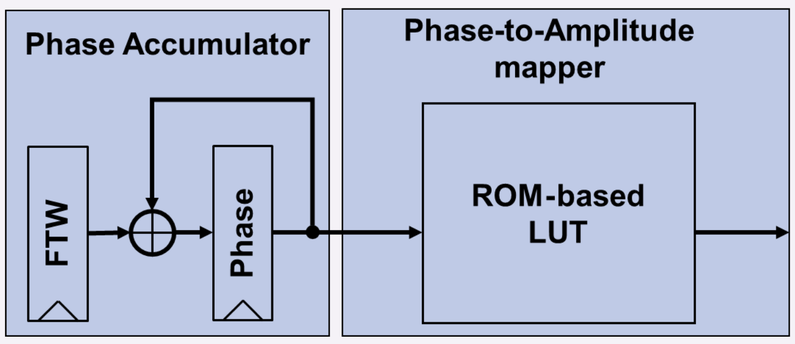
- **Definition**
  - Frequency synthesizer
  - Arbitrary waveform generator
- **Advantages**
  - Easy to manipulate frequency with high resolution

Objectives

- Research effect of Quarter method
  1) Power dissipation
  2) Area
  3) Timing constraint
- Research effect of Scaling-down CMOS technology (180nm & 65nm)

Operational principle comparison

❖ Conventional DDFS



DDFS Basic block

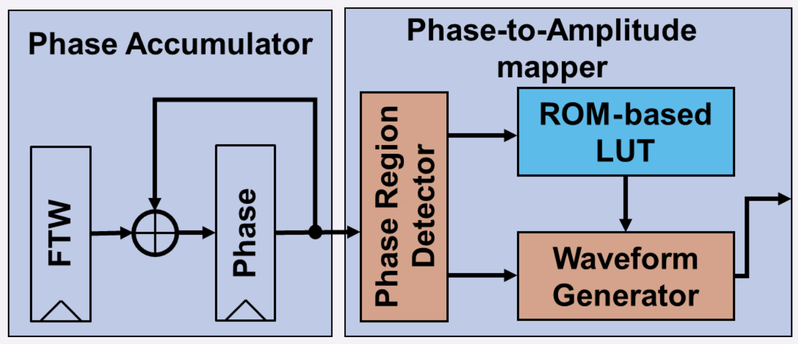
➢ **Phase Accumulator**

- Accumulate the phase by FTW (Frequency Tuning Word).
- FTW is arbitrary input that control the output frequency.

➢ **Phase-to-Amplitude Mapper**

- Appropriately translate the phase information to the amp. information.
- ROM-based LUT (Look-Up Table) stores amp. information corresponding to appropriate phase information.

❖ Quarter method of DDFS



Additional block

➢ **Phase Region Detector**

- Create indicator distinguishing the quadrature

➢ **Waveform generator**

- Reconstruct as a complete waveform

Reduced block

➢ **ROM-based LUT**

- Only store the quarter information of sine waveform

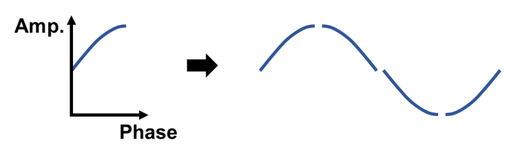
❖ The main formula

$$f_{out} = \frac{\mathrm{FTW} \times f_{clk}}{2^n}$$

f_{out}	Output frequency
f_{clk}	Clock frequency
n	Phase resolution
FTW	Frequency tuning word

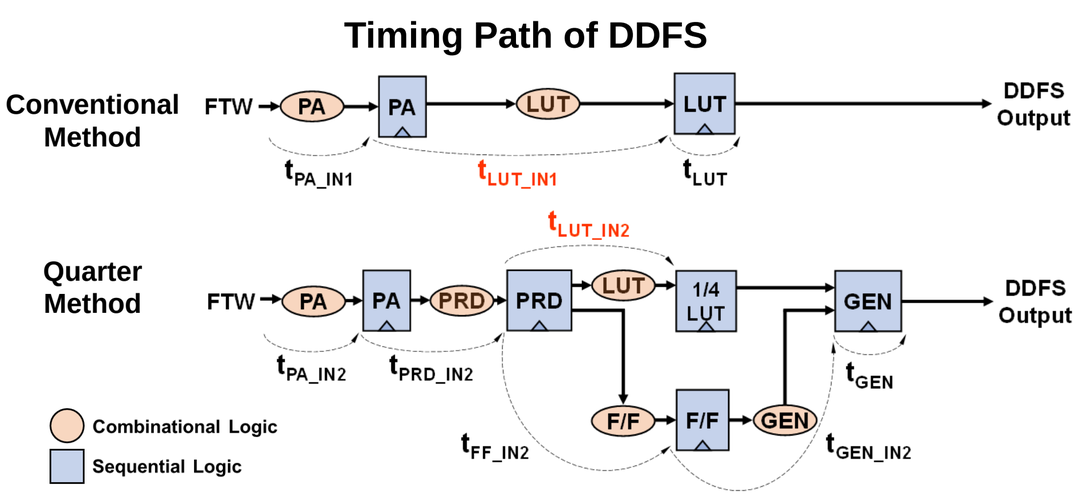
❖ Core of Quarter method

Symmetry & Periodicity of Sine waveform



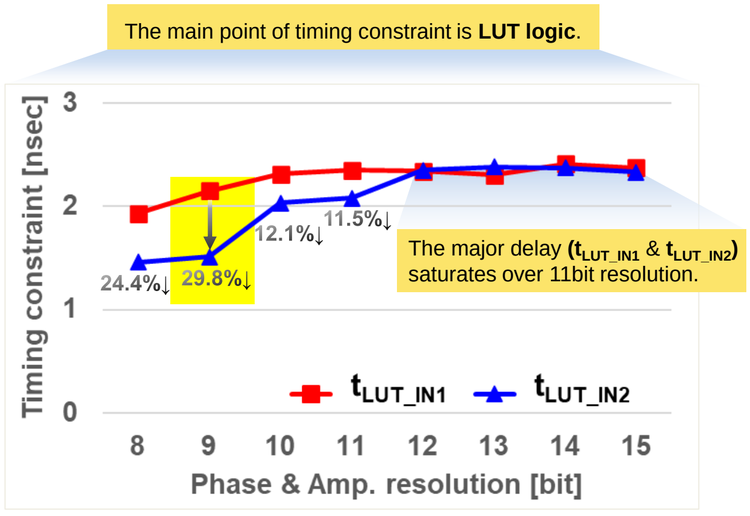
Timing constraint

Timing Path of DDFS



Resolution: 9 bits		
Conventional	t_{PA_IN1}	65 %
	t_{LUT_IN1}	100 %
	t_{LUT}	8 %
Quarter	t_{PA2_IN2}	65 %
	t_{PRD_IN2}	26 %
	t_{LUT_IN2}	70 %
	t_{FF_IN2}	9 %
	t_{GEN_IN2}	30 %
	t_{GEN}	8 %

* Low-Temperature case



Analysis summary

Conventional → Quarter

	Cell Area	Power Dissipation
180nm CMOS	66.92 % ↓	32.26 % ↓
65nm CMOS	62.25 % ↓	28.05 % ↓

* Resolution : 12 bits

180nm CMOS → 65nm CMOS

	Cell Area	Power Dissipation
Conventional	84.62 % ↓	77.15 % ↓
Quarter	82.45 % ↓	75.73 % ↓

* Resolution : 12 bits

➢ **Cell area is not reduced by a quarter. It's reduced by a third.**
(Additional blocks of quarter method exist.)

➢ **Scaling-down technology is highly efficient in large area.**

➢ **Quarter method is effective in cell area and power dissipation.**

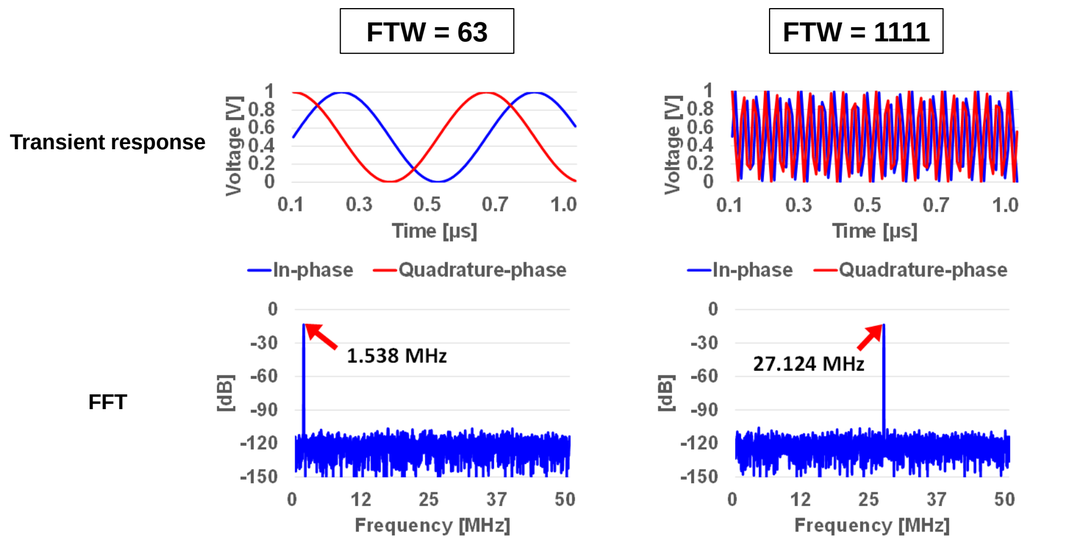
➢ **Scaling-down CMOS technology largely improves performance.**

Results

* Simulation is conducted by using ideal DAC and RTL code.

❖ Quarter Method

- $f_{clk} = 100\mathrm{MHz}$ • $n = 12$ bits



- Assumption : $f_{out} = 1.538\mathrm{MHz}$
- Simulation : $f_{out} = 1.538\mathrm{MHz}$
- Error rate : 0%

- Assumption : $f_{out} = 27.124\mathrm{MHz}$
- Simulation : $f_{out} = 27.124\mathrm{MHz}$
- Error rate : 0%

→ **Assumption = Simulation result**

Acknowledgement: This research was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education(2022R1A4A3029433111314820922601O1), and the Korea Institute for Advancement of Technology(KIAT) grant funded by the Korea Government(MOTIE) P0017011, HRD Program for Industrial Innovation).